IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Cohen et al.**

Serial No.: **09/377,642**

Filed: **August 19, 1999**

For: **Method and Apparatus for Performing Raster Operations in a Data Processing System**

§ Group Art Unit: **2671**

§

§ Examiner: **Tung, Kee M.**

§

§ Attorney Docket No.: **AT9-99-287**

§

Certificate of Mailing Under 37 C.F.R. § 1.8(a)
I hereby certify this correspondence is being deposited with the United States Postal Service as First Class mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231 on October 30, 2002.

By: Rebecca Clayton
Rebecca Clayton

TRANSMITTAL DOCUMENT

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:
ENCLOSED HEREWITH:

- Appellant's Brief (in triplicate) (37 C.F.R. 1.192); and
- Our return postcard.

A fee of $320.00 is required for filing an Appellant's Brief. Please charge this fee to IBM Deposit Account No. 09-0447. No additional fees are believed to be necessary. If, however, any additional fees are required, I authorize the Commissioner to charge these fees which may be required to Deposit Account No. 09-0447. No extension of time is believed to be necessary. If, however, an extension of time is required, the extension is requested, and I authorize the Commissioner to charge any fees for this extension to Deposit Account No. 09-0447.

Respectfully submitted,

Duke W. Yee
Registration No. 34,285
CARSTENS, YEE & CAHOON, LLP
P.O. Box 802334
Dallas, Texas 75380
(972) 367-2001
ATTORNEY FOR APPLICANTS

9/ Brief 11/6/02 1 of 3

Docket No. AT9-99-287 *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Cohen et al.** §

§ Group Art Unit: **2671**

Serial No. **09/377,642** §

§ Examiner: **Tung, Kee M.**

Filed: **August 19, 1999** §

§

For: **Method and Apparatus for Performing Raster Operations in a Data Processing System** §

Assistant Commissioner for Patents
Washington, D.C. 20231

ATTENTION: Board of Patent Appeals and Interferences

Certificate of Mailing Under 37 C.F.R. § 1.8(a)
I hereby certify this correspondence is being deposited with the United States Postal Service as First Class mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231 on October 30, 2002.

By: Rebecca Clayton
Rebecca Clayton

APPELLANT'S BRIEF (37 C.F.R. 1.192)

This brief is in furtherance of the Notice of Appeal, filed in this case on October 11, 2002.

The fees required under § 1.17(c), and any required petition for extension of time for filing this brief and fees therefore, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief is transmitted in triplicate. (37 C.F.R. 1.192(a))

REAL PARTIES IN INTEREST

The real party in interest in this appeal is the following party:

International Business Machines Corporation

RELATED APPEALS AND INTERFERENCES

With respect to other appeals or interference's that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal, there are no such appeals or interference's.

STATUS OF CLAIMS

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are: 1-32

B. STATUS OF ALL THE CLAIMS IN APPLICATION

1. Claims canceled: none
2. Claims withdrawn from consideration but not canceled: none
3. Claims pending: 1-32
4. Claims allowed: none
5. Claims rejected: 1-32

C. CLAIMS ON APPEAL

The claims on appeal are: 1-32

STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action.

SUMMARY OF INVENTION

The present invention provides a method and apparatus in a data processing system for performing a raster operation of graphics data. Specification, page 3, lines 3-5. A system memory and a video memory are included in the data processing system. Specification, page 3, lines 5-6. The system memory and the video memory are connected by a bus wherein the graphics data is organized into picture elements. Specification, page 3, lines 7-9. A plurality of picture elements is read from the system memory. Specification, page 3, lines 9-10. A plurality of picture elements is read from the video memory. Specification, page 3, lines 10-11. A raster operation is performed on the plurality of picture elements to form a plurality of processed picture elements. Specification, page 3, lines 11-13. The plurality of processed picture elements is written to the video memory. Specification, page 3, lines 13-15.

ISSUES

The issues on appeal are as follows:

1. Whether claims 1-6, 12-24, and 30 are anticipated by Noorbakhsh, U.S. Patent No. 5,699,498 ("*Noorbakhsh*") under 35 U.S.C. 102(b); and

2. Whether claims 7-11, 25-29, and 31-32 are unpatentable over Noorbakhsh, U.S. Patent No 5,699,498 in view of Brech, U.S. Patent No. 5,790,887 ("*Brech*") under 35 U.S.C. 103(a).

GROUPING OF CLAIMS

The claims stand and fall together as a single group.

ARGUMENT

I. 35 U.S.C. § 102, Anticipation, Claims 1-6, 12-24, and 30

With respect to the rejection of these claims, claim 1 is a representative claim of the claims rejected as being anticipated. Claim 1 reads as follows:

1. A method in a data processing system for performing a raster operation of graphics data, wherein the data processing system includes a system memory and a video memory, wherein the system memory and the video memory are connected by a bus and wherein the graphics data is organized into picture elements, the method comprising the data processing system implemented steps of:

selecting a first plurality of picture elements from the system memory;

selecting a second plurality of picture elements from the video memory, wherein the first plurality of picture elements and the second plurality of picture elements are selected such that changes in a direction of data on the bus are minimized when performing raster operations on the first plurality of picture elements and the second plurality of picture elements;

reading the first plurality of picture elements from the system memory;

reading the second plurality of picture elements from the video memory;

performing a raster operation on the first plurality of picture elements and the second plurality of picture elements to form a plurality of processed picture elements; and

writing the plurality of processed picture elements to the video memory, wherein changes in the direction of data on the bus are minimized between the reading and writing of picture elements.

In this particular case, each and every feature of the presently claimed invention is not shown in the same arrangement in *Noorbakhsh* as arranged in claim 1. A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983).

The portions of *Noorbakhsh* cited by the examiner teach a general raster operation, not the steps and the features within the steps as arranged in claim 1 of the present invention.

The examiner pointed to Figure 1 of *Noorbakhsh*, which is as follows:

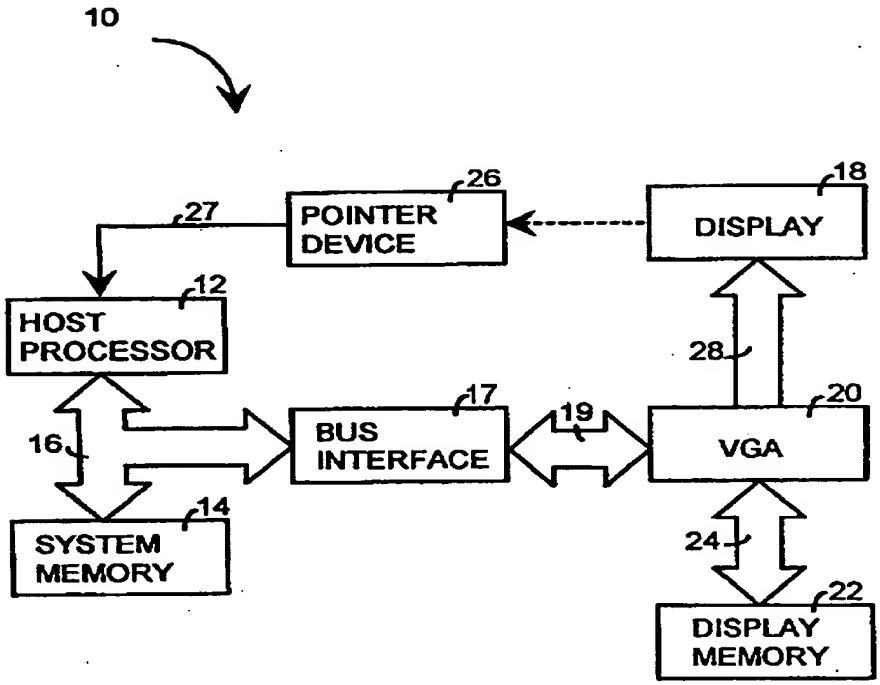

fig.1

As can be seen, Figure 1 of *Noorbakhsh* only discloses components used in displaying data. Nowhere does this figure teach the steps of the presently claimed invention in claim 1. In fact, no steps or processes are taught or disclosed by this figure.

The description of Figure 1 reads as follows:

> FIG. **1** illustrates, as an example, a block diagram of a computer system **10**. Included in the computer system **10** are a host processor **12** for performing certain processing functions, a display unit **18** and a pointer device **26** for facilitating user interaction with the host processor **12**, a video graphic adapter ("VGA") **20** for performing certain video processing and display control functions, and a bus interface **17** through which the host processor **12** communicates with the VGA controller **20**. Also included in the computer system **10** are system memory **14** and display memory **22** for storing, among other things, certain display data to be processed by the VGA controller **20**. A system bus **16** facilitates communication between the host processor **12**, the system memory **14**, and the bus interface **17**. Analog lines **27** facilitate communication between the pointing device and the host processor **12**. A subsystem bus **19** facilitates communication between the bus interface **17** and the VGA controller **20**. An internal memory bus **24** facilitates communication between the VGA

> controller **20** and the display memory **22**. An analog bus **28** facilitates communication between the VGA controller **20** and the display unit **18**.
>
> The host processor **12** is preferably one of a number of commercially available microprocessors such as those marketed, for example, by Intel and Motorola. The display unit **18** is preferably a VGA compatible color unit such as, for examples, certain cathode ray tubes ("CRTs") and liquid crystal displays ("LCDs"). The pointer device **26** is preferably a mouse or track ball type device suitable for pointing to locations on the display unit **18** and communicating signals indicative of those locations to the host processor **12**. The subsystem bus **19** may be any one of a number of buses such as an ISA, VESA.RTM. VL-Bus.TM., or Intel.RTM.-PCI bus.

Noorbakhsh, col. 9, lines 31-63. The description of this figure does not provide any further disclosure with respect to any of the steps recited in claim 1.

Next, the examiner cites to the following section of *Noorbakhsh* for performing a raster operation of the source and destination bitmap and for routing the results into a video memory:

> More particularly, a BitBLT operation comprises a sequence of steps including reading data from a source memory area and data from a destination memory area, logically combining the data respectively read from the source memory area and the destination memory area using one of a number of logical operations generally referred to as raster operations ("ROPs"), and writing the result of the logical operation into the destination memory area.

Noorbakhsh, col. 1, lines 24-31. This portion of *Noorbakhsh* teaches combining data and performing a raster operation. The data is then written back into a destination memory area. The steps of the present invention are not taught or suggested in this cited section of *Noorbakhsh*.

In the examiner's final Office Action, the examiner believes that the applicant is arguing that *Noorbakhsh* fails to read and write a plurality of pixel elements. This was not the argument made in the prior response. *Noorbakhsh* does not teach transferring pixels in the manner recited in claim 1.

More specifically, this cited section of *Noorbakhsh* fails to teach selecting the plurality of process picture elements to the video memory such that the direction of data on the bus is minimized between the reading and writing of the picture elements. This

particular feature is not shown in *Noorbakhsh*. The minimizing of changes in the direction of data on a bus through a selection of picture elements in claim 1 provides improved performance in processing graphics data. This feature is not found in *Noorbakhsh*. Such a feature is not merely the reading and writing of a plurality of picture elements, but involves selecting these elements in a manner such that changes in the direction of data on the bus are minimized when performing raster operations on the first plurality of picture elements and the second plurality of picture elements. Thus, the examiner has failed to consider all of the features of the presently claimed invention in asserting that anticipation is present based on *Noorbakhsh*.

Therefore, each and every feature of the presently claimed invention is not shown in *Noorbakhsh* in the same arrangement as in claim 1. As a result, *Noorbakhsh* does not anticipate claim 1. Consequently, the other independent claims having features similar to claim 1 also are patentable over *Noorbakhsh*. In addition, the dependent claims depend from one of the independent claims and are patentable over the cited reference for the same reason.

Thus, the rejection of claims 1-6, 12-24 and 30 under 35 U.S.C. § 102(b) should be reversed. In addition, these claims are not obvious in view of this cited reference.

No teaching, suggestion, or incentive is present in *Noorbakhsh* to modify the cited reference to select the process picture elements in a manner such that the direction of data on the bus is minimized between the reading and the writing of the picture elements from the different memories. The mere fact that *Noorbakhsh* could be modified to include such a feature does not make such a modification obvious.

Importantly, one of ordinary skill in the art would not be motivated to make such a modification when this reference is considered as a whole for what it teaches, rather than in a piecemeal fashion. *Noorbakhsh* is directed towards reducing the size of integrated circuits. In doing so, *Noorbakhsh* teaches the following:

> These and additional objects are accomplished by the various aspects of the present invention, wherein briefly stated, one aspect of the invention is a controller connected to a memory storing red, green, and blue color data for individual pixels of a display screen. Included in the controller are: means for storing data indicative of predefined shades of red, green, and blue; means for receiving monochrome color data for indicated pixels of the display screen; means for receiving red, green, and

blue color data from the memory, for the indicated pixels of the display screen; means for logically combining the received color data and corresponding ones of the predefined shades of red, green, and blue; and means for generating a plurality of column address strobe signals from the received monochrome color data such that the generated plurality of column address strobe signals cause the logically combined color data to replace stored red, green, and blue color data in the memory for selected ones of the indicated pixels as determined by the monochrome color data.

Another aspect of the invention is a method of performing a BitBLT operation on indicated pixels of a display screen, comprising: receiving data indicative of predefined shades of red, green, and blue; receiving monochrome color data for the indicated pixels of the display screen; receiving red, green, and blue color data from a memory, for the indicated pixels of the display screen; logically combining the received color data and corresponding ones of the predefined shades of red, green, and blue; and generating a plurality of column address strobe signals from the received monochrome color data such that the generated plurality of column address strobe signals cause the logically combined color data to replace stored red, green, and blue color data in the memory for selected ones of the indicated pixels as determined by the monochrome color data.

Still another aspect of the invention is a computer system comprising: a host processor; a display having a display screen with a number of pixels; a memory storing red, green, and blue color data for individual pixels of the display screen; and a controller. Included in the controller are: means for storing data indicative of predefined shades of red, green, and blue; means for receiving monochrome color data for indicated pixels of the display screen; means for receiving red, green, and blue color data from the memory, for the indicated pixels of the display screen, means for logically combining the received color data and corresponding ones of the predefined shades of red, green, and blue; and means for generating a plurality of column address strobes from the received monochrome data such that the generated plurality of column address strobes cause the logically combined color data to replace stored red, green, and blue color data in the memory for selected ones of the indicated pixels as determined by the monochrome color data.

Noorbakhsh col. 7, line 56 – col. 8, line 40. As can be seen, *Noorbakhsh* does not teach, suggest, or provide a motivation for a feature in which data from a system memory and video memory are selected for processing such that changes in the direction of the data on the bus are minimized between the reading and writing of the picture elements. Therefore, the presently claimed invention in the rejected claims can be reached only through an improper use of hindsight with the benefit of applicants' invention as a template for the needed changes.

II. 35 U.S.C. § 103, Obviousness, Claims 7-11, 25-29, and 31-32

A. The examiner bears the burden of establishing a *prima facie* case of obviousness.

The examiner bears the burden of establishing a *prima facie* case of obviousness based on the prior art when rejecting claims under 35 U.S.C. § 103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). In this particular case, the examiner has failed to establish a *prima facie* case of obviousness based on the prior art because (1) the examiner has failed to properly combine the references and (2) because the examiner has failed to consider all of the claim features recited in the claims. These reasons are described in more detail below.

B. A proper *prima facie* case of obviousness must be supported by some teaching or suggestion contained in the prior art.

A proper *prima facie* case of obviousness must be supported by some teaching or suggestion contained in the combined references. Applicants respectfully submit that the references cited cannot be combined to produce the claimed invention. The rule is:

> Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some **teaching, suggestion** or **incentive** supporting the combination.

In re Geiger, 815 F.2d 686, 688, 2 U.S.P.Q.2d 1276, 1278 (Fed. Cir. 1987)(emphasis added). In this case, no teaching, suggestion, or incentive has been given for combining these two references as proposed by the examiner. The examiner has only stated that it would be obvious to combine these references to avoid processor wait time and inefficient bus usage problems in the prior art system taught by *Brech*. In the final Office Action, the examiner pointed to the background section of *Brech* as providing the advantages and desirability of the modification proposed by the examiner. In actuality, when the background of *Brech* is considered, one of ordinary skill in the art would not combine *Brech* with *Noorbakhsh*.

The background of *Brech* is directed towards discussing problems associated with wait time and inefficient bus usage with respect to input/output bus operations in a computer system.

Noorbakhsh, however, is not concerned with such a problem. Instead, *Noorbakhsh* is more concerned with the following:

> In designing integrated circuits, it is an ongoing design goal to reduce the size of integrated circuits providing a given functionality. It is especially desirable to achieve such size reduction by reducing the complexity (or number of transistors) of the integrated circuitry performing the function or a comparable function.

Noorbakhsh col. 7, lines 40-45. As can be seen, when viewed by one of ordinary skill in the art, *Noorbakhsh* is more concerned with reducing the size of integrated circuits providing a particular functionality, rather than with problems associated with bus usage. Further, in reducing the size of circuits, *Noorbakhsh* is concerned more specifically with providing color expansion and byte alignment. For example, *Noorbakhsh* states the following:

> Accordingly, one object of the present invention is a BitBLT engine or accelerator including color expansion and byte alignment, or comparable functions, which is simpler in construction than prior art BitBLT engines including such functions.
>
> Another object is a BitBLT engine or accelerator including color expansion and byte alignment, or comparable functions, which is faster than prior art BitBLT engines including such functions.

Noorbakhsh, col. 7, lines 46-55.

Thus, *Brech* is concerned with problems associated with bus usage, while *Noorbakhsh* is concerned with reducing the complexity of circuits and in particular with providing color expansion and byte alignment functions in a BitBLT engine. Therefore, one of ordinary skill in the art would not be motivated to combine the teachings in these two references when they are considered as a whole.

Importantly, one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780, 1784 (Fed. Cir. 1992). One of ordinary skill in the art would consider the problems addressed by a reference to determine whether some teaching, suggestion, or incentive is present to support a combination.

In this particular case, the problems addressed by each of the references are different as well as the solutions. For example, *Noorbakhsh* is directed towards a VGA controller in a computer system described as follows:

> A computer system includes a host processor, a system memory, a display unit, a pointer device, a VGA controller, and a display memory. The VGA controller communicates with the display memory through an 8-byte wide data bus such that each byte is controlled by a separate column address strobe. To perform a BitBLT operation on a monochrome pattern to be logically combined with 888-RGB color-space formatted data in the display memory, the VGA controller includes a BitBLT control for generating numerous control signals; a color expand circuit for generating in response to such control signals, an 8-byte wide pattern of 888-RGB color-space formatted foreground color data; a circuit for logically combining in response to such control signals, the 8-byte wide pattern of 888-RGB color-space formatted foreground color data and a corresponding 8-byte wide pattern of 888-RGB color-space data received from the 8-byte wide data bus; a bit align circuit for generating in response to such control signals, column address strobe values indicative of bits of the monochrome pattern corresponding to the 8-byte wide pattern of 888-RGB color-space data received from the data bus, by bit aligning the bits of the monochrome pattern; and a memory sequencer for generating in response to such control signals, column address strobe signals corresponding to the values received from the bit align circuit, for strobing into the display memory selected bytes of the logically combined 8-bytes of data.

Noorbakhsh, Abstract.

On the other hand, *Brech* is more concerned with a method and apparatus for processing program input/output operations described as follows:

> A method and apparatus are provided for processing programmed input/output (PIO) operations in a computer system. A batched list of PIO operations is stored in a buffer. Then the batched list of PIO operations is moved as a single system bus operation to an I/O bus interface unit. The I/O bus interface unit includes sequencer logic. The sequencer logic is used for executing the batched list of PIO operations and for providing an ordered sequence of PIO operations to a system I/O bus. The method and apparatus of the invention enhances the use of non-intelligent I/O adapters in a computer system by reducing the overhead of system PIO operations. Also the correctly ordered sequence of PIO commands provided by the sequencer logic facilitates the use of non-intelligent I/O adapters in reduced instruction-set computer (RISC) systems.

Brech, Abstract. As can be seen, when these two references are considered as a whole for what they teach one of ordinary skill in the art, no teaching, suggestion, or incentive is present to support the combination.

This conclusion is further supported by consideration of other sections of these cited references. For example, Figure 1 of *Noorbakhsh* is as follows:

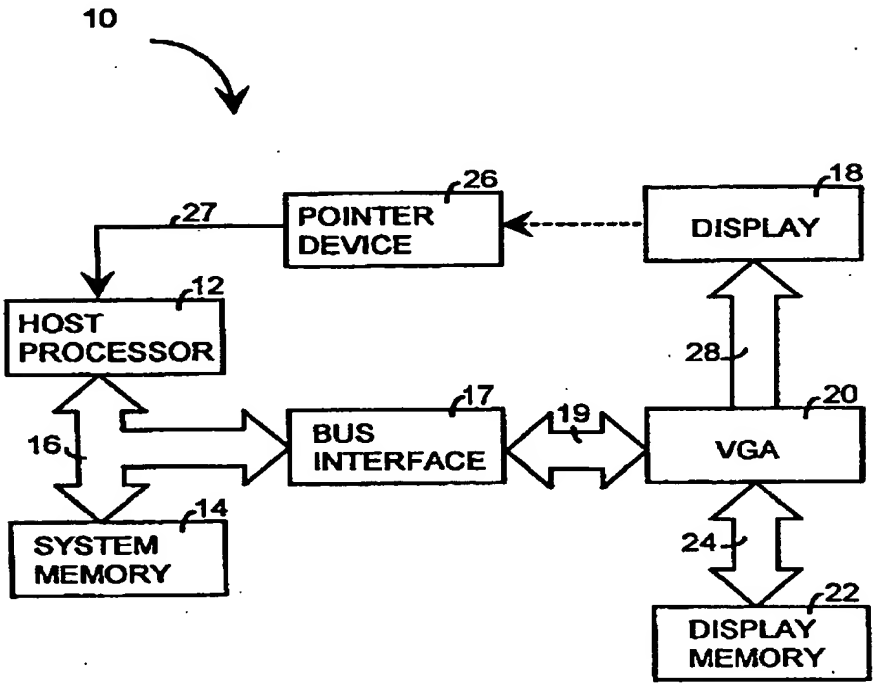

fig.1

Figure 10 of *Noorbakhsh* is as follows:

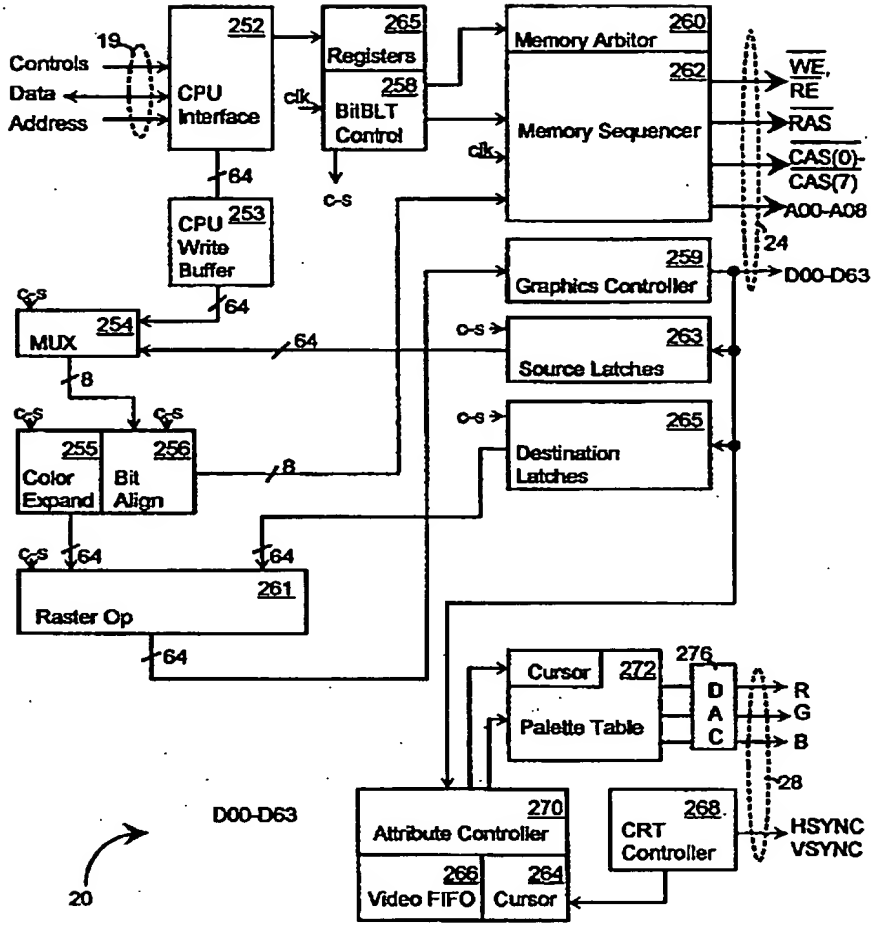

fig.10

Figure 10 is described as a block diagram of a VGA circuit utilizing aspects of the present invention in *Noorbakhsh*. As can be seen, the invention in *Noorbakhsh* is directed towards mechanisms located in VGA controller 20.

In contrast, *Brech* teaches a mechanism located in a different location within the computer system:

> In brief, a method and apparatus are provided for processing programmed input/output (PIO) operations in a computer system. A batched list of PIO operations is stored in a buffer. Then the batched list of PIO operations is moved as a single system bus operation to an I/O bus interface unit. The I/O bus interface unit includes sequencer logic. The sequencer logic used for executing the batched list of PIO operations and for providing an ordered sequence of PIO operations to a system I/O bus.

Brech, col. 2, lines 10-17. Figure 1A of *Brech* is as follows:

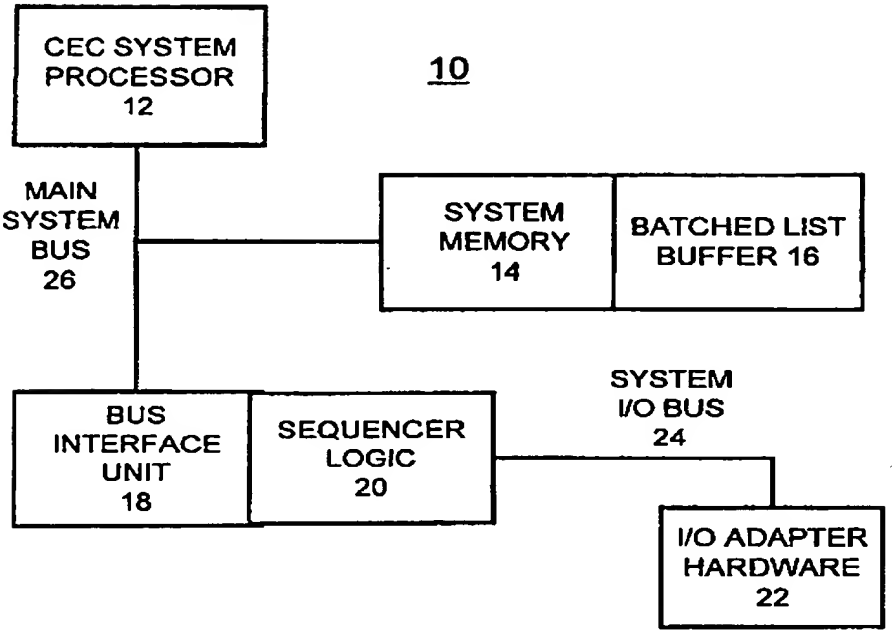

FIG.1A

The mechanisms of *Brech* are located in components other than a VGA adapter as taught by *Noorbakhsh*. In addition to teaching different locations for their mechanisms, *Brech* is not directed towards or concerned with color expansion or alignment processes as in *Noorbakhsh*. Thus, one of ordinary skill in the art would not be motivated to make the changes proposed by the examiner when these two references are fully considered by one of ordinary skill in the art.

Therefore, the claims rejected by these two references are patentable because these references cannot be combined as proposed by the examiner. Thus, these references cannot be combined absent an improper use of hindsight with the benefit of applicants' invention as a template to piece together the prior art.

C. All claim limitations must be considered, especially when missing from prior art.

The examiner has argued that the background of *Brech* teaches or suggests the advantages and desirability of the modification proposed by *Brech*. In comparing *Noorbakhsh* and *Brech* to the claimed invention, the claimed features of the present invention may not be ignored in an obviousness determination. The examiner's proposed modification does not take into account all of the features of the presently claimed invention.

Claim 7 is a representative claim of the claims rejected as being obvious in view of these two cited references. The present invention in claim 7 recites:

> 7. A method for performing raster operations in a graphics system, wherein the method comprises the data processing system implemented steps of:
>
> collecting a set of input operations into a batch of input operations substantially equal to a number of rasters in a video display; and
>
> sending the set of input operations on a video bus in a single operation.

In this particular case, the examiner has failed to consider that the input operations are collected into a batch of input operations substantially equal to a number of rasters in a video display. The examiner's rejection in the final Office Action does not take into account the feature in which input operations are collected into a batch of input operations substantially equal to a number of rasters in a video display. The examiner asserts that such a teaching or suggestion is present stating:

> Regarding 103 rejection, applicant argues that the combined system fails to suggest or teach, "the input operations are collected into a batch of input operations substantially equal to a number of rasters". The examiner disagrees with applicant because the feature reads by the teachings of Brech, such as, "a batched list (reads the collection of batches) of PIO operations is stored in a buffer. Then the batched list is moved as a single system bus operation to an I/O bus interface unit."

Office Action dated August 7, 2002, pages 3-4.

The Abstract of *Brech* reads as follows:

> A method and apparatus are provided for processing programmed input/output (PIO) operations in a computer system. A batched list of PIO operations is stored in a buffer. Then the batched list of PIO operations is moved as a single system

> bus operation to an I/O bus interface unit. The I/O bus interface unit includes sequencer logic. The sequencer logic is used for executing the batched list of PIO operations and for providing an ordered sequence of PIO operations to a system I/O bus. The method and apparatus of the invention enhances the use of non-intelligent I/O adapters in a computer system by reducing the overhead of system PIO operations. Also the correctly ordered sequence of PIO commands provided by the sequencer logic facilitates the use of non-intelligent I/O adapters in reduced instruction-set computer (RISC) systems.

Brech, Abstract. Although the Abstract teaches placing programmed input/output (PIO) operations into a batched list, the Abstract fails to teach the specific features of claim 7. The collecting step in claim 7 collects a set of input operations into a batch of input operations substantially equal to the number of rasters in a video display. In other words, the batch of input operations is a set of input operations that is substantially equal to the number of rasters in a video display. No such teaching, suggestion, or incentive is present in this cited portion of *Brech*. Instead, *Brech* teaches using sequencer logic for executing PIO operations without any mention as to how these PIO operations are placed on a batched list.

No such teaching or suggestion is present in either reference alone or in combination. Although *Brech* may suggest grouping operations, no teaching, suggestion, or incentive is present to motivate one of ordinary skill in the art to group them in the manner recited in these claims.

"It is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art." *In re Hedges*, 228 U.S.P.Q. 685, 687 (Fed. Cir. 1986). A review of *Brech* provides no further teaching, suggestion, or incentive for batching input operations such that a set of input operations forms a batch input operations substantially equal to a number of rasters in a video display.

Moreover, in reviewing *Brech* as a whole, one of ordinary skill in the art would find this reference to teach away from the presently claimed invention in claim 7. Specifically, *Brech* teaches:

> Referring to FIG. **3**, there is shown a flow chart illustrating the method of the invention for processing PIO operations in the computer system **10**. The sequential steps begin at a block **300** to process an I/O device interrupt by CEC system processor **12**. For example, multiple PIO reads may be added to the PIO queue. A batch I/O element is created and added to the batch I/O list buffer **16** by the CEC system processor **12** as indicated at a block **302**. It is determined by CEC system processor **12** whether more I/O operations are required as indicated at a decision block **304**, for example, for each of the multiple reads. If yes, then a next I/O element is created and added to the batch I/O list buffer **16** by CEC system processor **12**. When no additional I/O operations are required, an execute batch I/O function is called by the CEC system processor **12** as indicated at a block **306**. Then the batch I/O list is moved to the sequencer logic **20**,...

Brech, col. 4, lines 36-51. This portion of *Brech* teaches batching PIO reads together as a group. The I/O operations are reviewed to determine whether they are part of the multiple reads. Such a teaching teaches away from collecting input operations into a batch of input operations substantially equal to a number of rasters in a video display.

The examiner has failed to take this particular feature into account in combining *Noorbakhsh* with *Brech*. Therefore, a combination of *Noorbakhsh* and *Brech*, even if proper, would not reach the presently claimed invention.

D. Stating that it is obvious to try or make a modification or combination without a suggestion in the prior art is not *prima facie* obviousness.

The mere fact that a prior art reference can be readily modified does not make the modification obvious unless the prior art suggested the desirability of the modification. *In re Laskowski*, 871 F.2d 115, 10 U.S.P.Q.2d 1397 (Fed. Cir. 1989) and also *see In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992) and *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1993). The examiner may not merely state that the modification would have been obvious to one of ordinary skill in the art without pointing out in the prior art a suggestion of the desirability of the proposed modification. The mere fact that the examiner could modify *Brech* to collect the input operations into a batch of input operations substantially equal to a number of rasters in a video display does not make such a modification obvious. The modification cannot be made without some teaching, suggestion, or incentive for this particular

modification. The sections cited by the examiner provide no such teaching, suggestion, or incentive.

Instead, these sections have only been cited for the proposition that a batch list of operations is moved as a single bus operation. The examiner has not pointed out any teaching, suggestion, or incentive for collecting a set of input operations into a batch of input operations substantially equal to a number of rasters in a video display and then sending that set of input operations on a video bus in a single operation. Therefore, a *prima facie* case of obviousness has not been made with respect to *Brech*. In fact, *Brech* actually teaches away from this type of collecting of input operations when other portions of *Brech*, in addition to those cited by the examiner, are reviewed by one of ordinary skill in the art. Further, *Noorbakhsh* also provides no teaching, suggestion, or incentive for such a modification. As a result, a combination of these two references, even if proper, would not reach the presently claimed invention.

Therefore, it is respectfully requested that the rejection of the claims be reversed.

Duke W. Yee
Reg. No. 34,285
Carstens, Yee & Cahoon, LLP
PO Box 802334
Dallas, TX 75380
(972) 367-2001

APPENDIX OF CLAIMS

The text of the claims involved in the appeal is:

1. A method in a data processing system for performing a raster operation of graphics data, wherein the data processing system includes a system memory and a video memory, wherein the system memory and the video memory are connected by a bus and wherein the graphics data is organized into picture elements, the method comprising the data processing system implemented steps of:

selecting a first plurality of picture elements from the system memory;

selecting a second plurality of picture elements from the video memory, wherein the first plurality of picture elements and the second plurality of picture elements are selected such that changes in a direction of data on the bus are minimized when peforming raster operations on the first plurality of picture elements and the second plurality of picture elements;

reading the first plurality of picture elements from the system memory;

reading the second plurality of picture elements from the video memory;

performing a raster operation on the first plurality of picture elements and the second plurality of picture elements to form a plurality of processed picture elements; and

writing the plurality of processed picture elements to the video memory, wherein changes in the direction of data on the bus are minimized between the reading and writing of picture elements.

2. The method of claim 1, wherein the plurality of processed picture elements form a scan line.

3. The method of claim 1, wherein the raster operation performs a logic OR function using a picture element from the system memory and a picture element from the video memory.

4. The method of claim 1, wherein the first plurality of picture elements are part of a source bitmap.

5. The method of claim 1, wherein the second plurality of picture elements are part of a destination bitmap.

6. The method of claim 1, wherein the reading steps, the performing step, and the writing step are performed in a graphics engine.

7. A method for performing raster operations in a graphics system, wherein the method comprises the data processing system implemented steps of:

collecting a set of input operations into a batch of input operations substantially equal to a number of rasters in a video display; and

sending the set of input operations on a video bus in a single operation.

8. The method of claim 7 further comprising:

collecting a set of output operations into a batch of output operations substantially equal to a number of rasters in a video display; and

sending the set of output operations on a video bus in a single operation.

9. The method of claim 7, wherein the set of input operations are sent to a system memory connected to a video bus.

10. The method of claim 7, wherein the set of output operations are sent to a video memory connected to a video bus.

11. A method for performing raster operations in a graphics system, wherein the method comprises the data processing system implemented steps of:

collecting a set of output operations into a batch of input operations substantially equal to a number of rasters in a video display; and

sending the set of output operations on a video bus in a single operation.

12. A data processing system comprising:

a bus;

a system memory connected the bus, wherein a first plurality of graphics elements are located within the system memory;

a video memory connected to the bus, wherein a second plurality of graphics elements are located within the video memory;

a processor unit connected to the bus, wherein the processor unit executes instructions to select a first plurality of picture elements from the system memory; select a second plurality of picture elements from the video memory in which the first plurality of picture elements and the second plurality of picture elements are selected such that changes in a direction of data on the bus are minimized when performing raster

operations on the first plurality of picture elements and the second plurality of picture elements; read the first plurality of picture elements from the system memory; read the second plurality of picture elements from the video memory; perform a raster operation on the first plurality of picture elements and the second plurality of picture elements to form a plurality of processed picture elements; and write the plurality of processed picture elements to the video memory in which changes in the direction of data on the bus are minimized between the reading and writing of picture elements.

13. The data processing system of claim 12, wherein the first plurality of graphics elements is a plurality of picture elements.

14. The data processing system of claim 12, wherein the first plurality of graphics elements form a scan line.

15. The data processing system of claim 12, wherein the scan line is a scan line in a bitmap.

16. The data processing system of claim 13, wherein the first plurality of picture elements form a bitmap.

17. The data processing system of claim 12, wherein a graphics engine performs the raster operation.

18. The data processing system of claim 12, wherein a video driver performs the raster operation.

19. A data processing system for performing a raster operation of graphics data, wherein the data processing system includes a system memory and a video memory, wherein the system memory and the video memory are connected by a bus and wherein the graphics data is organized into picture elements, the data processing system comprising:

first selecting means for selecting a first plurality of picture elements from the system memory;

second selecting means for selecting a second plurality of picture elements from the video memory, wherein the first plurality of picture elements and the second plurality of picture elements are selected such that changes in a direction of data on the bus are minimized when performing raster operations on the first plurality of picture elements and the second plurality of picture elements;

reading means for reading the first plurality of picture elements from the system memory;

reading means for reading the second plurality of picture elements from the video memory;

performing means for performing a raster operation on the first plurality of picture elements and the second plurality of picture elements to form a plurality of processed picture elements; and

writing means for writing the plurality of processed picture elements to the video memory, wherein changes in the direction of data on the bus are minimized between the reading and writing of picture elements.

20. The data processing system of claim 19, wherein the plurality of processed picture elements form a scan line.

21. The data processing system of claim 19, wherein the raster operation performs a logic OR function using a picture element from the system memory and a picture element from the video memory.

22. The data processing system of claim 19, wherein the first plurality of picture elements are part of a source bitmap.

23. The data processing system of claim 19, wherein the second plurality of picture elements are part of a destination bitmap.

24. The data processing system of claim 19, wherein the first reading means, the second reading means, the performing means, and the writing means are located in a graphics engine in the data processing system.

25. A data processing system for performing raster operations in a graphics system, wherein the data processing system comprises:

collecting means for collecting a set of input operations into a batch of input operations substantially equal to a number of rasters in a video display; and

sending means for sending the set of input operations on a video bus in a single operation.

26. The data processing system of claim 25 further comprising:

collecting means for collecting a set of output operations into a batch of output operations substantially equal to a number of rasters in a video display; and

sending means for sending the set of output operations on a video bus in a single operation.

27. The data processing system of claim 25, wherein the set of input operations are sent to a system memory connected to a video bus.

28. The data processing system of claim 25, wherein the set of output operations are sent to a video memory connected to a video bus.

29. A data processing system for performing raster operations in a graphics system, wherein the data processing system comprises:

collecting means for collecting a set of output operations into a batch of input operations substantially equal to a number of rasters in a video display; and

sending means for sending the set of output operations on a video bus in a single operation.

30. A computer program product in a computer readable medium for performing a raster operation of graphics data, wherein the data processing system includes a system memory and a video memory, wherein the system memory and the video memory are connected by a bus and

wherein the graphics data is organized into picture elements, the computer program product comprising:

first instructions for selecting a first plurality of picture elements from the system memory;

second instructions for selecting a second plurality of picture elements from the video memory, wherein the first plurality of picture elements and the second plurality of picture elements are selected such that changes in a direction of data on the bus are minimized when performing raster operations on the first plurality of picture elements and the second plurality of picture elements;

third instructions for reading the first of a first plurality of picture elements from the system memory;

fourth instructions for reading the second plurality of picture elements from the video memory;

fifth instructions for performing a raster operation on the first plurality of picture elements and the second plurality of picture elements to form a plurality of processed picture elements; and

sixth instructions for writing the plurality of processed picture elements to the video memory, wherein changes in the direction of data on the bus are minimized between the reading and writing of picture elements.

31. A computer program product in a computer readable medium for performing raster operations in a graphics system, wherein the computer program product comprises:

first instructions for collecting a set of input operations into a batch of input operations substantially equal to a number of rasters in a video display; and

second instructions for sending the set of input operations on a video bus in a single operation.

32. A computer program product in a computer readable medium for performing raster operations in a graphics system, wherein the computer program product comprises:

first instructions for collecting a set of output operations into a batch of input operations substantially equal to a number of rasters in a video display; and

second instructions for sending the set of output operations on a video bus in a single operation.